Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE**

**.030 x .030”**

**.040”**

**.040”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .030 x .030”**

**Backside Potential: CATHODE**

**APPROVED BY: DK DIE SIZE .040” X .040” DATE: 9/2/21**

**MFG: MICROSEMI / PPC THICKNESS .000” P/N: 1N5802**

**DG 10.1.2**

#### Rev B, 7/1